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DOC

The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(54) Method of manufacturing a thin film transistor.

(57) In a process for manufacturing a thin film transistor, a first polysilicon layer (9) is formed on a substrate (10) and a silicon dioxide layer (11) is formed on a region of the first polysilicon layer leaving exposed regions of that layer. A second polysilicon layer (12) is formed on the silicon dioxide layer and aligned therewith. Regions of a selectively-grown electrically-conductive film (13) are deposited on the second polysilicon layer and on the exposed regions (14,15) of the first polysilicon layer, the film being such that it will not grow on the edges (16,17) of the silicon dioxide layer, but will grow on the exposed polysilicon to form gate (18), source (19) and drain (20) electrodes. The edges of the silicon dioxide layer therefore remain uncoated. The film may be formed of tungsten or may be formed, for example, by selective silicon expitaxy, phosphorus doped.

Fig.2(a).

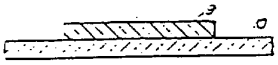


Fig.2(b).

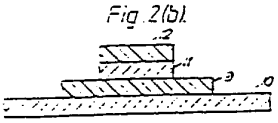


Fig.2(c).

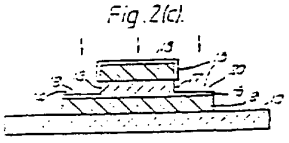
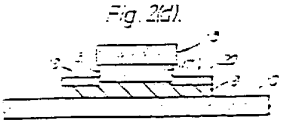


Fig.2(d).



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Description

Semiconductor Devices

This invention relates to the manufacture of thin film transistors (TFTs) by the deposition of polysilicon.

Figure 1 of the accompanying drawings illustrates the first steps in a well-known process for the formation of a polysilicon TFT. Firstly, a layer (Figure 1(a)) of silicon dioxide is deposited on a glass substrate 2. A layer 3 of polysilicon is then formed over a region of the silicon dioxide layer. A further area 4 (Figure 1 (b)) of silicon dioxide is formed on the layer 3, and a gate region 5 of polysilicon is formed in alignment with the area 4. The gate region 5 and regions 6 and 7 of the layer 3 projecting beyond the gate region are then doped (Figure 1 (c)) by ion implantation to form gate, source and drain regions respectively, of n^+ polysilicon. Contact layers (not shown) are subsequently formed over the regions. During the ion implantation process, the gate region 5 acts as a mask, which should prevent doping of the central region 8 of the layer 3. However, unless very careful control over the ion implantation process is maintained, the doped regions 6 and 7 will extend underneath the gate region 5, forming parasitic capacitances between the gate and the source and between the gate and the drain. The capacitances will reduce the speed of the operation of the device.

Furthermore, the ion implantation process accounts for a major part of the cost of forming the device. Moreover, ion implantation is not suitable for the production of TFTs over a large area.

In an alternative known process, (not shown), the lower silicon dioxide layer is covered with a mask having apertures through which doped source and drain regions similar to the regions 6 and 7 are deposited. A layer of polysiliocn is formed over those regions, followed by a silicon dioxide layer. A gate region similar to the region 5 is then formed centrally on the silicon dioxide layer. There is a considerable likelihood that the gate region will overlap the edges of the source and drain regions, and parasitic capacitances such as mentioned above will result.

It is an object of the present invention to provide a process for manufacturing polysilicon TFTs which does not involve the use of ion implantation to produce the conductive regions, and in which the production of the above-mentioned parasitic capacitances is avoided.

According to the invention there is provided a process for manufacturing a thin film transistor, including the steps of forming a first polysilicon layer on a substrate; forming a silicon dioxide layer on a region of the first polysilicon layer leaving exposed regions of said first polysilicon layer; forming a second polysilicon layer on the silicon dioxide layer and aligned therewith; and depositing on the second polysilicon layer and on the exposed regions of the first polysilicon layer, regions of a selectively-grown electrically-conductive film, which film will not grow on the edges of the silicon dioxide layer but will grow on the exposed polysilicon.

Preferably the electrically-conductive film is formed of tungsten.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Figure 1 illustrates steps in a known TFT manufacturing process as described hereinbefore, and

Figure 2 illustrates corresponding steps in a process in accordance with the invention.

Referring to Figure 2(a), a layer 9 of polysilicon is formed on a substrate 10. A layer 11 (Figure 2(b)) of silicon dioxide is formed over a region of the layer 9, and a layer 12 of polysilicon is formed over the layer 11 and in alignment therewith. The device is then heated in a chemical vapour deposition chamber so that a substrate temperature of around 350°-450° C is achieved. Tungsten hexafluoride is introduced into the chamber. A conductive layer 13 (Figure 2(C)) of tungsten is thereby selectively-grown on the layer 12 and on the exposed regions 14 and 15 of the layer 9. It is found, however, that the film 13 does not grow on the edges 16, 17 of the silicon dioxide film, which therefore remain uncoated.

The film therefore forms a conductive gate electrode 18 and conductive source and drain electrodes 19, 20 which are isolated from each other and the edges of which would be exactly aligned with each other if it were not for the portion of the layer 13 on the vertical edges of the layer 12. However, that layer is extremely thin, so that there is no appreciable overlapping of the regions to constitute the above-mentioned parasitic capacitances.

The device can be subsequently heated to cause the tungsten to diffuse into the upper surfaces of the polysilicon layers 9 and 12, as show in Figure 2(d).

Although deposition of tungsten by a chemical vapour deposition technique is described above, any conductive material may be deposited by any method in which the material will grow on the polysilicon but not on the edges of the silicon dioxide layer. For example, selective silicon epitaxy, phosphorus-doped, may be used.

It will be apparant that the expensive conventional ion implantation process is not required in the process of the present invention.

Claims

1. A process for manufacturing a thin film transistor, characterised by the steps of forming a first polysilicon layer (9) on a substrate (10); forming a silicon dioxide layer (11) on a region of the first polysilicon layer leaving exposed regions (14,15) of said first polysilicon layer; forming a second polysilicon layer (12) on the silicon dioxide layer and aligned therewith; and depositing on the second polysilicon layer and on the exposed regions of the first polysilicon layer, regions (18,19,20) of a selec-

tively-grown electrically-conductive film (13), which film will not grow on the edges (16,17) of the silicon dioxide layer but will grow on the exposed polysilicon.

2. A process as claimed in Claim 1, characterised in that the electrically-conductive film (13) is a layer of tungsten.

3. A process as claimed in Claim 2, characterised in that the deposition step comprises introducing tungsten hexafluoride gas into an evacuated chamber containing the substrate (10) with the polysilicon and silicon dioxide layers (9,12,11) thereon.

4. A process as claimed in Claim 3, characterised in that during the deposition step the temperature of the substrate (10) is maintained in the range of 350° to 450° C.

5. A process as claimed in any preceding claim, characterised in that after the deposition of the film (13), the substrate (10) with said layers (9,12,11) and film (13) thereon is heated to cause diffusion of the material of the film into the regions (14,15) of the first polysilicon layer (19) and into the second polysilicon layer (12).

Fig. 1(a).

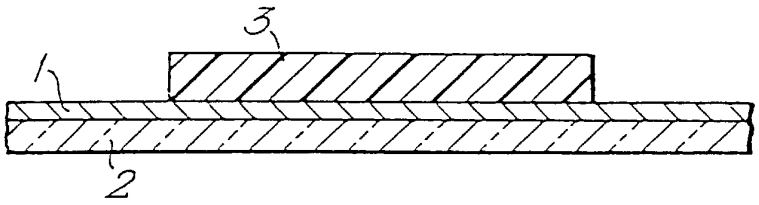


Fig. 1(b).

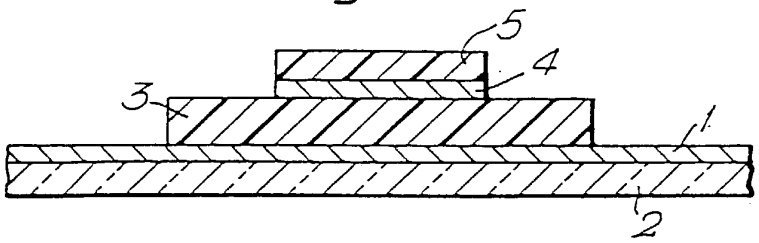


Fig. 1(c).

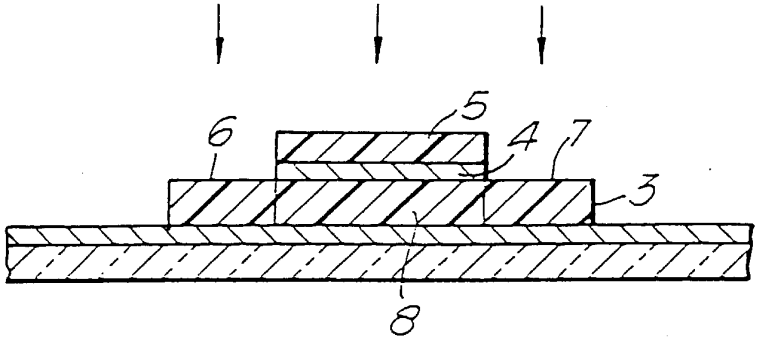


Fig.2(a).

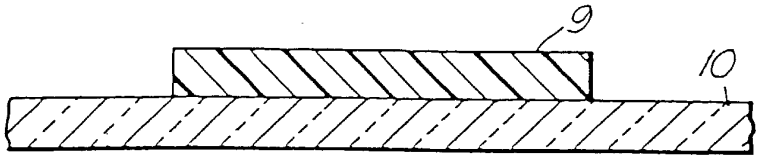


Fig.2(b).

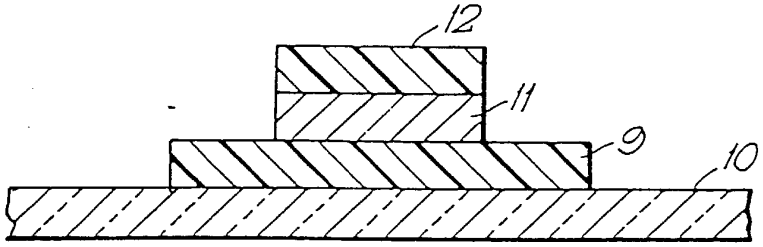


Fig.2(c).

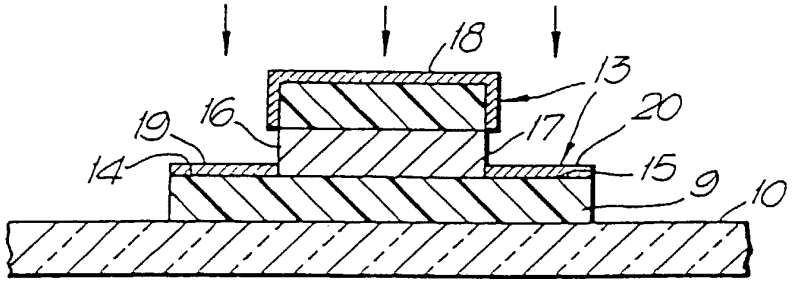
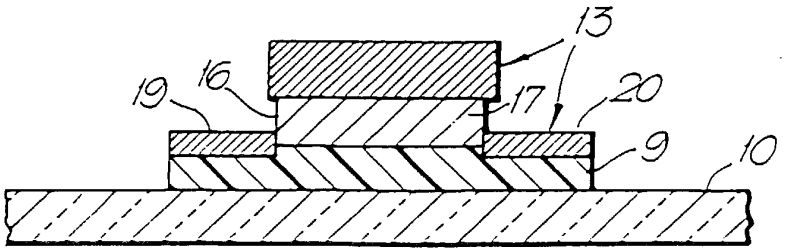


Fig.2(d).



European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 1591

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 24, no. 7b, December 1981, NEW YORK US pages 3640 - 3641; S.W.DEPP et al.: "Method of fabricating FET in polycrystalline silicon" * the whole document *	1	H 01 L 21/84 H 01 L 21/285 H 01 L 29/78 H 01 L 21/90
A	EP-A-0 147 913 (K.K.TOSHIBA) * page 6, line 23 - page 7, line 10; figures 4A-4D *	2-4	
A	US-A-4 330 931 (SHEAU-MING S.LIU)		
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY. vol. 131, no. 6, June 1984, MANCHESTER, NEW HAMP pages 1427 - 1433; E.K.BROADBENT et al.: "Selective Low Pressure Vapor Deposition of Tungsten"		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	21 November 90	ZOLLFRANK G.O.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document

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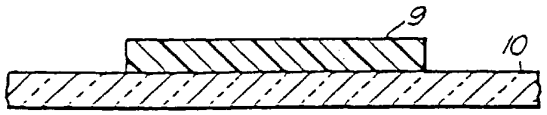

Fig.2(b).

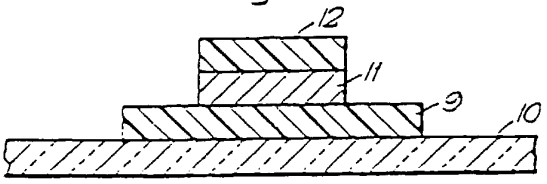

Fig. 2(c).

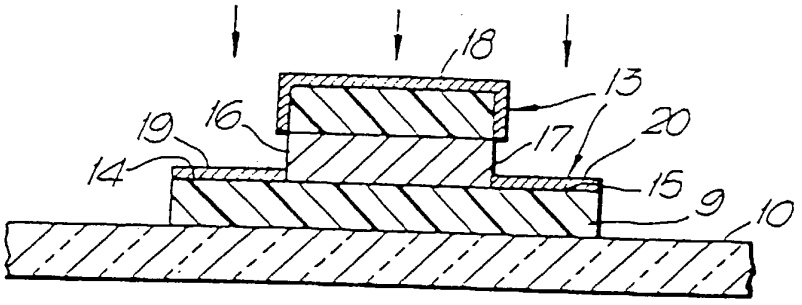

Fig. 2(d).